ABSTRACT

The present invention describes a two transistor flash EEPROM memory cell which has a symmetrical source and drain structure, which permits the cell size not limited by program and erase operations. The memory cell comprises an NMOS floating gate transistor forming a nonvolatile storage device and an NMOS transistor forming an access device. The floating gate transistor is programmed and erased using Fowler-Nordheim channel tunneling. The two transistor memory cell is used in a memory array of columns and rows where a column of cells is coupled by a bit line and a source line, and where a row of cells is coupled by a word line and an access line. The memory array is highly scalable and is targeted for low-voltage, high-speed and high-density programmable logic devices.